AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A process for connecting processed semiconductor wafers, wherein at least two processed semiconductor wafers are located in a mid position of a stack of wafers, and wherein in an operation of a mechanical connecting, electrically insulating connections and electrically conductive connections are produced between said at least two processed semiconductor wafers each one thereof having a wafer surface side to be connected, said process comprising:

applying ~~structured~~ patterned layers of an electrically non-conducting glass paste and an electrically conducting glass paste on ~~two~~ said wafer surface sides ~~of said two wafers to be connected~~;

conditioning and premelting of the electrically non-conducting glass pastes and the electrically conducting glass paste;

geometrical alignment of the at least two processed semiconductor wafers to be connected;

joining the at least two processed semiconductor wafers at a processing temperature of the ~~glass pastes~~ electrically non-conducting glass paste and the electrically conducting glass paste using a mechanical pressure.

2. (Currently Amended) The process according to claim 1, wherein the ~~glass pastes~~electrically non-conducting glass paste and the electrically conducting glass paste are applied by a screen printing process.

3. (Currently Amended) The process according to claim 1, wherein ~~that~~ the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions and, therefore, the conditioning process and the premelting process are implemented successively, each in a ~~in a~~ separate conditioning and premelting process.

4. (Currently Amended) The process according to claim 1, wherein ~~that~~ the electrically non-conducting glass paste and the electrically conducting glass paste have ~~substantially~~ the same processing temperature.

5. (Currently Amended) The process according to claim 1, wherein the electrically non-conductive glass paste and the electrically conducting glass paste have different processing temperatures and ~~these~~ wherein the processing temperatures are successively passed in ~~a~~ the process for connecting the at least two processed semiconductor wafers.

6. (Currently Amended) The process according to claim 1, wherein at least one of the at least two processed semiconductor wafers ~~is~~ has an ~~electrically connected~~ electrical connection in an area that ~~is~~ does not contain electronic structures~~structured electronically as an area of a starting material of the wafer~~.

7. (Currently Amended) The process according to claim 1, wherein the at least two processed semiconductor wafers are electrically connected at specific electric circuit points in ~~electronically structured~~ areas containing electronic structures.

8. (Currently Amended) The process according to claim 1, wherein ~~a connection formation of~~joining the at least two processed semiconductor wafers by the electrically non-conducting glass paste and the electrically conducting ~~the~~ glass pastes takes place at a processing temperature in a range of 450°C.

9. (Currently Amended) The process according to claim 1, wherein ~~the electric connection of a substrate of an~~ one of the at least two processed semiconductor wafers is a SOI wafer comprising an active semiconductor layer and a buried oxide layer on a substrate and wherein an electrical connection to the substrate of the SOI wafer is implemented through previously produced openings in ~~a~~ the buried oxide layer and in ~~an~~ the active ~~silicon~~ semiconductor layer.

10. (Cancelled)

11. (Withdrawn) A process for bonding processed semiconductor wafers as system wafer supporting micro-electromechanical or electronic structures with a cover wafer also supporting electronic structures, wherein in an operation of bonding, electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers, said process comprising:

applying a first electrically non-conducting, structured layer and a second electrically conducting structured layer, each one with a glass paste on at least one face of the wafers to be bonded together,

conditioning of the glass pastes;

geometrical alignment of the wafers to be bonded;

joining the wafers together at a processing temperature of the glass pastes using a mechanical pressure.

12. (Withdrawn) The process according to claim 11, wherein the glass pastes are applied with a screen printing process.

13. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different premelting condition and premelting of each of the pastes is implemented successively in a separate process.

14. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a substantially same processing temperature.

15. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different processing temperatures.

16. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected in a wafer area not structured electronically.

17. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected at a specific electric circuit point located in an electronically structured area of the wafer.

18. (Withdrawn) The process according to claim 11, wherein a glass paste connection formation takes place at a temperature of less than 450°C.

19. (Withdrawn) The process according to claim 11, wherein the electric connection of a substrate of an SOI wafer is implemented through at least one previously produced opening in a buried oxide layer of said SOI wafer and in an active silicon layer, of said SOI wafer whereby at least one wall area of the at least one opening in the active silicon layer being provided with an insulating layer prior to the electric connection with the conducting glass paste.

20. (Cancelled)

21. (New) The process according to claim 1, wherein applying first patterned layer of the electrically non-conducting glass paste to the wafer surface side of one of the at least two processed semiconductor wafers and a second patterned layer of the electrically conducting glass paste on the wafer surface side of other of the at least two processed semiconductor wafers.